

3-Bit Binary Counter With Astable Multivibrator As Clock Circuit

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Abstract:

I supposed to propose 3 bit binary counter with astable multivibrator as a clock circuit. This circuit contains astable multivibrator and a 3-bit asynchronous binary down counter. This counter contains three T-flip-flops. Astable multivibrator contains one operational amplifier IC741, Capacitor, three Resistors and power supply to produce V_{sat} voltage. Total eight states and all states repeat for every eight clock pulses. Initial state is 000 and after applying clock the state is decremented by 1.

Reference Circuit Details:

Astable multivibrator is designed by using capacitor of capacitance 10nF, two resistors R_1 , R_2 of resistance of $1K\Omega$, and negative feedback resistor of resistance $4.5K\Omega$.

$$\text{Now, feedback factor } \beta = \frac{R_2}{R_1 + R_2} = \frac{1k\Omega}{2k\Omega} = 0.5$$

$$\tau = 2R_f C \ln \left(\frac{1+\beta}{1-\beta} \right)$$

$$f = \frac{1}{\tau} = \frac{1}{(2.2)(4.5 \times 10^3)(10^{-8})} = 10\text{KHz}$$

Astable multivibrator produces clock to counter with 10KHz frequency. Fig-2 shows the output of the astable multivibrator which is input to the counter as a clock.

Consider V_{sat} as logic high and $-V_{sat}$ as logic low. Output of Astable multivibrator is connected as clock of flipflop T_0 , output of T_0 is connected as clock of T_1 , and output of T_1 is connected as clock of T_2 . T_0 , T_1 , T_2 are connected to V_{sat} (logic high) for toggling.

For every positive edge of clock delivered by astable multivibrator, T_0 gets toggled. For every positive edge of output of T_0 , T_1 gets toggled. For every positive edge of output of T_1 , T_2 gets toggled.

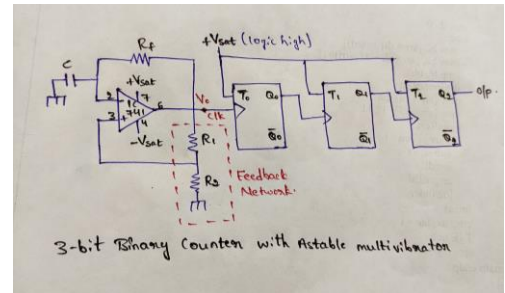


Figure 1

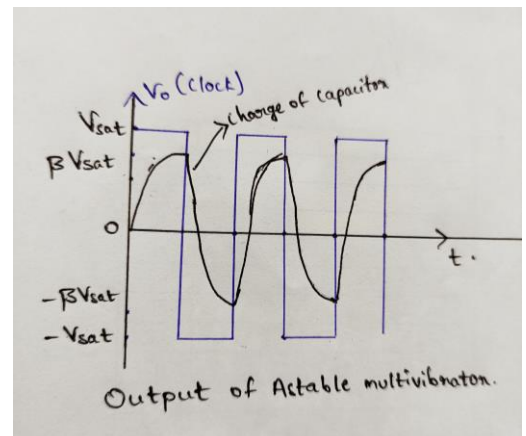


Figure 2

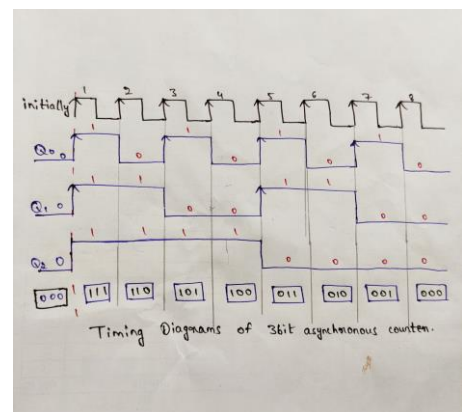


Figure 3